ABSTRACT OF THE DISCLOSURE

A gate wire including a plurality of gate lines and gate electrodes in the display area, and gate pads in the peripheral area is formed on a substrate having a display area and a peripheral area. A gate insulating layer, a semiconductor layer, an ohmic contact layer and a conductor layer are sequentially deposited, and the conductor layer and the ohmic contact are patterned to form a data wire including a plurality of data lines, a source electrode and a drain electrode of the display area and data pads of the peripheral area, and an ohmic contact layer pattern thereunder. A passivation layer is deposited and a positive photoresist layer is coated thereon. The photoresist layer is exposed to light through one or more masks having different transmittance between the display area and the peripheral area. The photoresist layer is developed to form a photoresist pattern having the thickness that varies depending on the position. At this time, a thin portion and a thick portion of the photoresist pattern are provided for the display area, and a thick portion and a zero thickness portion for the peripheral area. In the peripheral area, the portions of the passivation layer, the semiconductor layer and the gate insulating layer on the gate pads, and the portions of the passivation layer on the data pads, under the zero thickness portion, are removed. In the display area, the thin portion of the photoresist pattern, and the portions of the passivation layer and the semiconductor layer thereunder are removed but the portions of the passivation layer under the thick portions of the photoresist pattern is not removed. Then, a plurality of pixel electrodes, redundant gate pads and redundant data pads are formed.